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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/615,134

07/08/2003

Waldemar Brinkis

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27799 7590 07/31/2007  
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EXAMINER

RODELA, EDUARDO A

ART UNIT

PAPER NUMBER

2826

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/615,134	<b>Applicant(s)</b> BRINKIS ET AL.	
	<b>Examiner</b> Eduardo A. Rodela	<b>Art Unit</b> 2826	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 April 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 4/27/07 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>4/27/07</u> .   | 6) <input type="checkbox"/> Other: _____                          |

### DETAILED ACTION

This Office Action is in response to Amendment filed April 27, 2007.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattman et al. (EP 1 249 869) in view of Asai et al. (US 4,521,476) in further view of Liederbach (US 3,714,709) in further view of Honda (US 5,245,510).

Regarding claim 1, Mattmann shows an electronics unit, comprising:

a low multi-point metallic mount [1];

an insulating layer [2] arranged on said mount;

a conductor track system [4,5,6,7, which is a thick film type conductor, see English abstract] on said insulating layer [2];

a resistance layer [9, made of thick film paste as stated in english abstract] disposed on the polymer layer within one area of the conductor track [4,5,6,7].

Mattmann does not show an insulating layer comprises a sintered electrically insulating polymer layer and also does not specify the conductor track system is comprised of a sintered glass frit with a noble metal filling. Asai shows (e.g. Figures 5-8) an insulating layer comprises a sintered [it is well known in the art that epoxies are cured by the application of heat, see line 7 of paragraph 0030 of Sakamoto et al. (US

2002/0020554)) electrically insulating polymer layer [1, which is used to connect conductor tracks 3' to metal base 8]. Asai teaches the benefits of having an insulating layer which is comprised of a sintered electrically insulating polymer layer as a material which can be used to permit high heat conductivity [column 2: line 60 to column 3: line 4]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the insulating layer comprising a sintered electrically insulating polymer layer arranged on said mount in the invention of Mattman as suggested by Asai because the insulating layer can be used to permit high heat conductivity. Liederbach shows an electronic system which has a conductor track system [4,6,8,10,12,14] is comprised of a sintered glass frit with a noble metal filling [column 3: lines 8-31]. Liederbach teaches the benefit of using a conductor track system is comprised of a sintered glass frit with a noble metal filling to allow for screen printing pattern transfer [column 2: lines 55-65]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the conductor track system is comprised of a sintered glass frit with a noble metal filling in the invention of Mattmann as suggested by Liederbach to allow for screen printing pattern transfer.

Even though Mattman shows the thick film resistor, which could be interpreted to be an electronic power components, for the purposes of the new limitation creating the need for the prior art to exhibit an additional power component beyond the originally claimed component, Mattman does not show the additional component. Honda shows in Figure 1, the semiconductor device [5] connecting to a thick film resistor [9] by a conductor track [8], which additionally has a plurality of electronic power devices

[10,11]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have included a plurality of power components in the invention of Mattman in view of Asai, in further view of Liederbach as suggested by Honda, for the purpose of providing more functionality to the overall package such as signal conditioning, logic, etc.

It is noted that the limitations of the resistance layer being "printed" is considered to be a process limitation that carries no patentable weight because the current claim is directed to a device structure, therefore a "product by process" claim is directed to the product, and no matter how the structure is actually made, it is the final product which must be determined in a "product by process" claim, and not the patentability of the process. The presence of process limitations on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. *In re Stephens* 145 USPQ 656 (CCPA 1965).

Regarding claim 2, Mattmann /Asai/Liederbach/Honda show the electronics unit of claim 1. Liederbach, wherein said noble metal filling comprises one of a silver filling and a filling containing silver [column 3: lines 8-31]. It is noted that this claim does not further limit the claim on which it depends.

Regarding claim 3, Mattmann /Asai/Liederbach/Honda show the electronics unit of claim 1. In addition, Liederbach shows wherein said glass frit is a low melting-point glass frit [shows the use of borosilicate glass frit, column 3: lines 22-27, which is well known to be a low melting point glass, see column 7: lines 18-27 of Pryor et al. (US 4,821,151)].

Regarding claim 4, Mattmann /Asai/Liederbach/Honda show the electronics unit of claim 2. In addition, Liederbach shows wherein said glass frit is a low melting-point glass frit [shows the use of borosilicate glass frit, column 3: lines 22-27, which is well known to be a low melting point glass, see column 7: lines 18-27 of Pryor et al. (US 4,821,151)].

Regarding claim 5, Mattmann /Asai/Liederbach/Honda show the electronics unit of claim 1. In addition, Mattmann shows wherein said mount [1] is made of a material from the group consisting of aluminum and an aluminum alloy [see English abstract].

Regarding claim 6, Mattmann /Asai/Liederbach/Honda show the electronics unit of claim 1. In addition, Mattmann shows wherein said mount [1] comprises cooling ribs [protrusions on bottom surface].

Regarding claim 7, Mattmann /Asai/Liederbach/Honda show the electronics unit of claim 1. In addition, Mattmann shows wherein said power components [3] comprise at least one of power semiconductor elements and driver components [see English abstract].

Regarding claim 8, Mattmann /Asai/Liederbach/Honda show the electronics unit of claim 1. In addition, Mattmann shows comprising at least one of electrical and electronic components [9] arranged on the conductor track system [between 6 and 7].

Regarding claim 9, Mattmann /Asai/Liederbach/Honda show the electronics unit of claim 8. In addition, Mattmann shows wherein said power components [3] and said

at least one of electrical and electronic components [9] are conductively connected to the conductor track system by bonding [both are bonded to conductor tracks 4,6,7].

Regarding claim 10, Mattmann /Asai/Liederbach/Honda show the electronics unit of claim 1. In addition, Mattmann shows wherein said power components [3] and said at least one of electrical and electronic components [9] are conductively connected to the conductor track system by bonding [both are bonded to conductor tracks 4,6,7].

Regarding claim 11, Mattmann /Asai/Liederbach/Honda show the electronics unit of claim 1. In addition, Asai shows wherein said electrically insulating polymer layer [1] has a thickness of about >20 um [column 4: lines 52-55].

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mattman et al. (EP 1 249 869) in view of Asai et al. (US 4,521,476) in further view of Liederbach (US 3,714,709) in further view of Honda (US 5,245,510) in further view of Akram (US 6,417,027).

Regarding claim 12, Mattmann /Asai/Liederbach/Honda show the electronics unit of claim 1. Mattmann /Asai/Liederbach/Honda do not show:

a further insulating layer comprising a sintered polymer arranged on said conductor track system and on said electronic power components; a further conductor track system comprising a sintered glass frit with noble metal filling arranged on said further insulating layer; and further electronic power components arranged on said further conductor track system. Akram shows (e.g. Figures 1-4 and 8) a further insulating layer comprising a sintered polymer [insulator portion of 12, column 4: lines 23-35, uses polyimide, which is well known as a thermosetting material, see column 9:

lines 24-29 of Meissner et al. (US 5,264,326)] arranged on a conductor track system [25] and on electronic power components [14]; a further conductor track system [portion of 12, made of conductive polymer thick film, column 4: lines 46-52]; and

further electronic power components [14, column 4: lines 15-25] arranged on said further conductor track system [12]. Akram teaches the benefits of stacking insulators, conductor tracks, and extra devices to facilitate high density stacking of semiconductor devices [column 1: lines 15-18] as suggested by Akram. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the further insulating layer comprising a sintered polymer arranged on said conductor track system and on said electronic power components; a further conductor track system arranged on said further insulating layer; and further electronic power components arranged on said further conductor track system in the invention of Mattmann /Asai/Liederbach/Honda as suggested by Akram in order to facilitate high density stacking of semiconductor devices. Akram does not show the specific constituents of the polymer thick film conductor track system. However, Liederbach discloses that sintered glass frit with a noble metal filling is a known material for conductive polymer thick films. The applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

***Response to Arguments***



Applicant's arguments filed April 27, 2007 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Art Unit: 2826

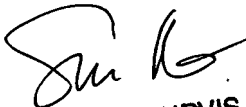
***Fax / Telephone Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A. Rodela whose telephone number is (571) 272-8797. The examiner can normally be reached on M-F, 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eduardo A Rodela  
Examiner  
Art Unit 2826

  
SUE A. PURVIS  
SUPERVISORY PATENT EXAMINER

*E. A. R.*